11.3 A Multi-Standard Analog and Digital TV Tuner for Cable and Terrestrial Applications

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Broadband television and data reception has gained more attention in recent years mainly due to the advent of new digital TV standards and improved content such as high-definition television. At the same time, modern TV tuners in the United States, Europe, and much of the rest of the world must still receive legacy analog broadcasts until at least 2009 for terrestrial applications and probably longer for cable broadcasts.

A typical cable TV spectrum has a limited input power range with small undesired-to-desired-signal (U/D) ratios, but contains a large number of channels resulting in possible distortion products [1,2]. Terrestrial, or off-air, TV spectrums have relatively few channels compared to cable, but they can have a wide range of input powers with the possibility of very large U/D ratios. For example, according to the North American digital television specification (ATSC A/74), there can be an interferer 6 channels (36MHz) away that has 57dB higher power than the desired signal [3]. Classically, both the tuner RF and IF AGC functions have been controlled by the demodulator, which only sees the desired channel and has no knowledge of interferers. This is acceptable for cable applications where the shape of the rest of the input spectrum can be inferred from the power of the desired signal. However, narrow tracking filters have not yet been integrated on silicon tuners, and there is a large frequency range of signals present at the input of the tuner active circuitry. The large interferer cannot be effectively filtered out on chip. Therefore, the tuner must provide its own RF AGC function to prevent compression, while letting the demodulator to control the IF AGC. Even the narrow tracking filters of discrete canned tuners have trouble attenuating such a large interferer. Many modern canned digital tuners need self-contained RF AGC control.

The goal of the presented tuner is to use AGC to optimize the power levels at every block in the signal path. This provides the best possible RF performance by maximizing the input power, and therefore, the SNR, into every block without causing excessive distortion. By optimizing the signal path gain lineup in this way, the AGC does not need to distinguish between desired and undesired power levels. To accomplish this, a simple power detector with a few dB of range is required after every change in signal bandwidth (i.e., filtering), and gain control is provided at several locations in the signal path. Figure 11.3.1 shows the block diagram of the tuner. It is a dual-conversion architecture with external first- and second-IF SAW filters, and it consists of an input buffer and attenuator, a variable gain single-ended-input to differential-output LNA, an upconversion mixer, a variable gain image-reject downconversion mixer, an IF VGA, two fractional-N frequency synthesizers, two hybrid power/peak detectors, and a master AGC control block.

All RF gain control is done in small digital steps controlled from up/down counters. As long as the step size is kept small enough, it causes no burst errors for digital signals and the step is invisible to the eye for analog signals. To prevent the AGC from running continuously, it shuts itself down when the desired power levels are reached. This prevents the digital gain control from toggling between two values. If the measured power moves outside of a reference power window, as in the case of dynamic multipath signal fading, the AGC will turn itself back on and re-center the power levels. The overall AGC update frequency and the desired power level at each power/peak detector are programmable to accommodate different modulation standards and input situations (cable versus off-air).

The hybrid rms power/peak detector is shown in Fig. 11.3.2. The signal is first rectified and then low-pass filtered to a bandwidth of about 8MHz. This removes the instantaneous peaks caused by phase addition of several input channels, which could lead to the detector not settling. The filtered signal is then sent to a simple peak detector with adjustable bleed current to handle time variations between peaks in different modulation schemes.

The digitally programmable front-end attenuator is preceded by an emitter follower to buffer it from the source impedance, which may not be well defined in televisions using low-cost antennas. It consists of a MOSFET switched resistive divider with careful design of the series and shunt resistance values to keep both the noise figure and the input-referred distortion on a 1dB/dB versus attenuation slope. If the input resistance is too low, it can cause distortion in the input emitter follower. Conversely, if the output resistance is too high, it can cause noise problems due to the large base current shot noise from the following stage. Furthermore, the percentage of FET switch resistance to real resistance in each leg has been optimized to prevent distortion from the FETs.

The LNA is a cascoded and degenerated differential pair with one input AC grounded through an off-chip capacitor to provide single-ended to differential conversion. Its load resistors are digitally programmable in fine steps to provide gain control. Since cable applications specify a maximum return loss of –6dB, the input to the chip has digitally programmable shunt resistors to provide the input match. This allows the tuner to trade the best terrestrial input sensitivity for better input return loss when switching between terrestrial and cable inputs. Both mixers are current-commutating (Gilbert cell) double-balanced configurations, and the downconversion image-reject mixer also contains digitally programmable gain control. The IF VGA is an analog voltage-controlled current-steering amplifier with over 40dB of gain range [4]. Both LOs are fractional-N synthesizers utilizing a mixture of CMOS and CML logic. The VCOs are standard cross-coupled LC tank bipolar topologies. The tanks consist of digitally switched NFETs for coarse frequency tuning, accumulation-mode varactors for analog fine tuning, and bondwire tank inductors.

The measured input sensitivity of the tuner and the required specification for terrestrial ATSC signals are shown in Fig. 11.3.3. Figure 11.3.4 shows the tuner performance for a weak desired ATSC signal in the presence of large undesired analog interferers. The U/D mask requirements are taken from the ATSC specification [3]. In Fig. 11.3.5, the tuner performance in a fully loaded cable system is plotted, including composite triple beat (CTB), composite second order (CSO), AM cross-modulation (XMOD), and carrier-to-noise ratio (CNR) in a 6MHz signal bandwidth. The test consists of 131 analog channels with 100% amplitude modulation at an input power of 15dBmV (-32dBm) per channel. Typical analog requirements for CTB, CSO, XMOD, and CNR are –63dBc, –60dBc, –57dBc, and 52dB, respectively. Figure 11.3.6 shows a table of measured results. The chip consumes 1.5W from a split 5V and 3.3V supply, and the die size is 7.29mm^2. It is fabricated in a 0.35µm SiGe BiCMOS process and a die micrograph is shown in Fig. 11.3.7.

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References:
[1] K. Simons, "The Decibel Relationships Between Amplifier Distortion Products," *Proc. IEEE,* vol. 58, no. 7, pp. 1071-1086, July, 1970.
[2] Matrix Technical Notes MTN-109, "The Relationship of Intercept Points and Composite Distortions," April, 1997.
[3] ATSC A/74, "ATSC Recommended Practice: Receiver Performance Guidelines," Advanced Television Systems Committee, June, 2004.
[4] A. Schneider and O. Werther, "Nonlinear Analysis of Noise in Current-Steering Variable Gain Amplifiers," *IEEE J. Solid-State Circuits,* vol. 39, pp. 290-296, Feb., 2004.

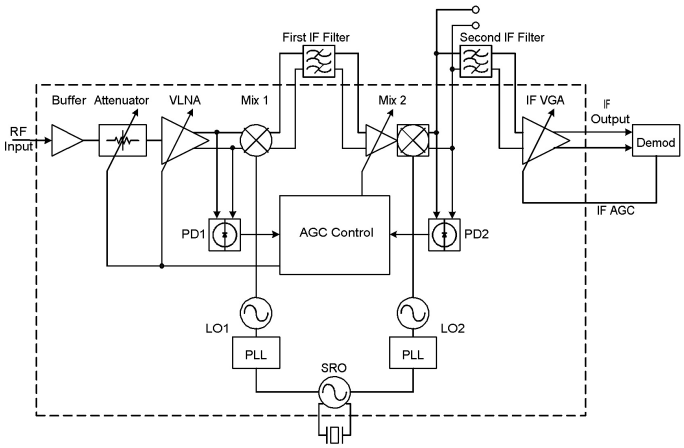

Figure 11.3.1: Block diagram of the tuner.

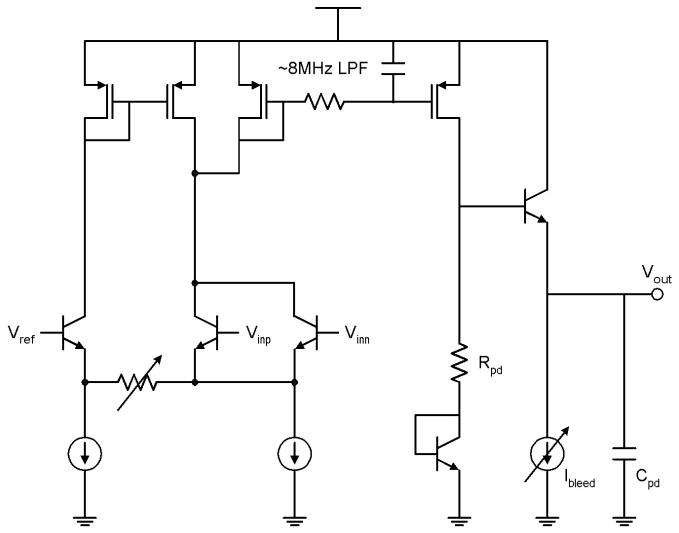

Figure 11.3.2: Schematic of the hybrid power/peak detector.

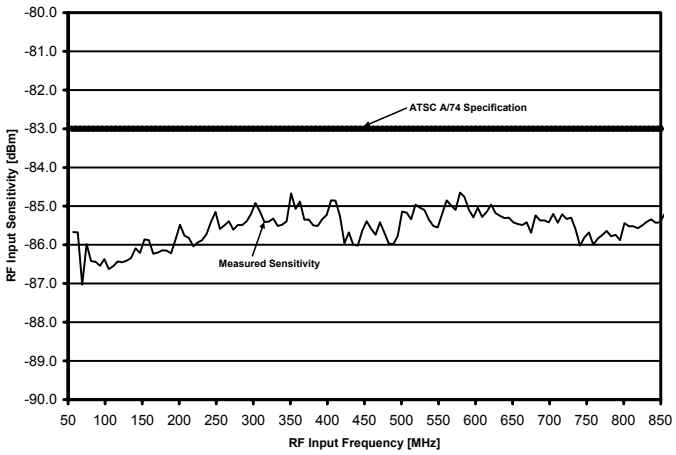

Figure 11.3.3: Measured ATSC input sensitivity of the tuner.

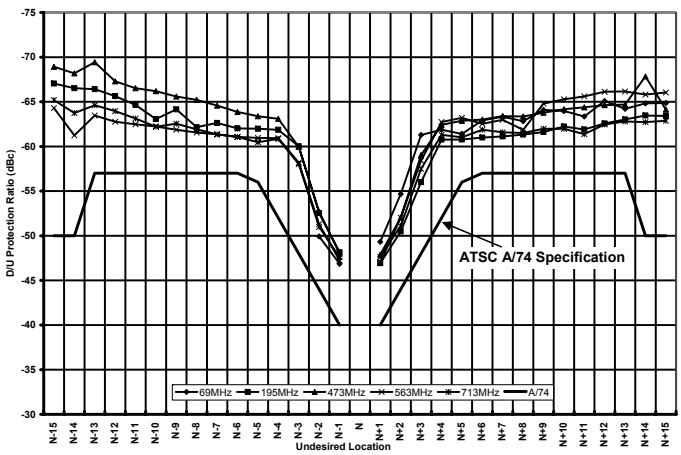

Figure 11.3.4: Measured D/U protection ratio for analog interference in ATSC.

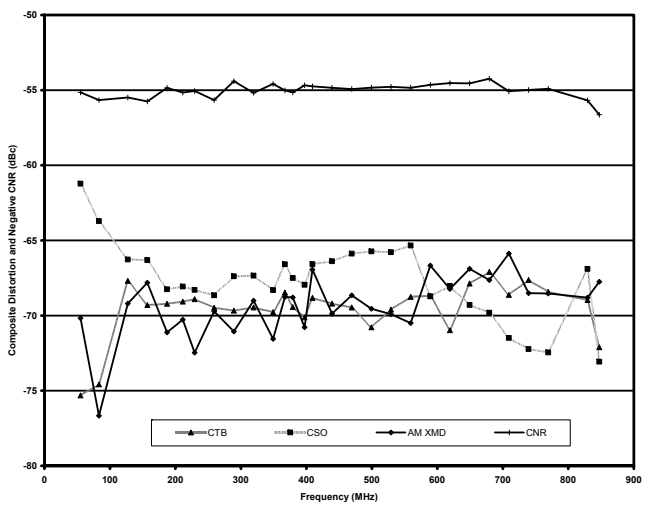

Figure 11.3.5: Composite distortion and CNR of the tuner.

Parameter	DVB-T Terrestrial	ISDB-T Terrestrial	ATSC Terrestrial	Analog Terrestrial	Analog and Digital Cable
Input frequency range (MHz)	48 to 862	48 to 862	48 to 862	48 to 862	48 to 1000
RF AGC range	55dB				
Noise Figure (Max Gain)	6dB	6dB	6dB	6dB	8dB
IIP3 (Max Gain)	+2dBm	+2dBm	+2dBm	+2dBm	+5dBm
IIP3 (25dB Attenuation)	+30dBm	+30dBm	+30dBm	+30dBm	+30dBm
Image rejection	75dB				
LO phase noise (10 kHz)	-85dBc/Hz				
LO phase noise (100 kHz)	-105dBc/Hz				
Sensitivity	-82dBm	-82dBm	-85dBm	-	-
N±1 Max Interferer	>35dBc	-	>47dBc	-	-
N±4 Max Interferer	>47dBc	-	>60dBc	-	-
CTB	-	-	-	-	<-65dBc
CSO	-	-	-	-	<-60dBc
XMOD	-	-	-	-	<-65dBc
Active Current (5V Supply)	250mA				
Active Current (3.3V Supply)	80mA				
Die Size	2.7mm x 2.7mm				

Figure 11.3.6: Performance summary.

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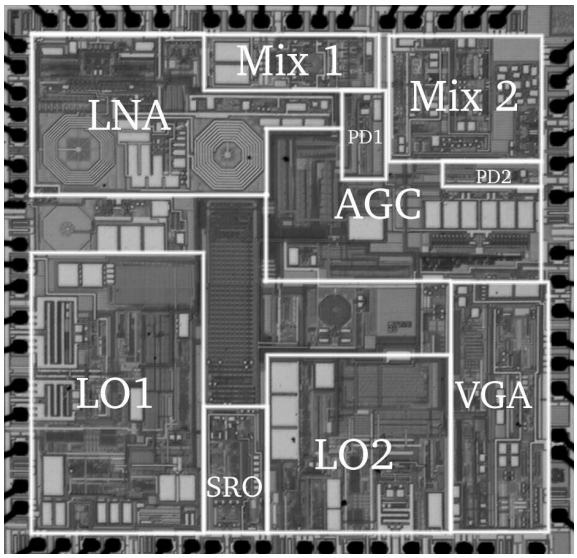

Figure 11.3.7: Die micrograph.

